What is claimed is:

1. A semiconductor apparatus having a delay monitor circuit for perceiving critical path delay characteristics of a target circuit, wherein:

said delay monitor circuit comprises

a delay means having a plurality of delay elements for forming delay element arrays in accordance with supplied configuration information including a delay component to cause signal propagation delay inside said target circuit;

a plurality of registers to be set a plurality of configuration information for forming said delay element arrays; and

a switching means for selectively switching the configuration information of said plurality of registers and supplying to said delay means.

2. A semiconductor apparatus as set forth in claim 1, wherein said switching means switches configuration information of delay element arrays set in the plurality of registers in a time sharing way and supplies to said delay means.

3. A semiconductor apparatus as set forth in

claim 2, wherein said delay monitor circuit comprises a control means for controlling a power source voltage to be supplied to said target circuit based on delay information generated by a delay element array formed in a time sharing way.

4. A semiconductor apparatus as set forth in claim 3, wherein said control circuit compares a plurality of delay information generated by a plurality of delay element arrays formed in the above delay means, judges delay information with the largest delay value as final delay information and controls said power source voltage based on the final delay information.

5. A semiconductor apparatus having a delay monitor circuit for perceiving critical path delay characteristics of a target circuit including a plurality of circuits operating at different clock frequencies, wherein:

said delay monitor circuit comprises

a delay means having a plurality of delay elements for forming delay element arrays in accordance with supplied configuration information including a delay component to cause signal propagation delay inside said target circuit;

a plurality of registers to be set a plurality of configuration information for forming said delay element arrays in accordance with said plurality of different frequencies;

a first switching means for selectively switching the configuration information of said plurality of registers and supplying to said delay means; and

a second switching means for selectively switching said plurality of clocks and supplying to said delay means.

6. A semiconductor apparatus as set forth in claim 5, wherein:

said first switching means switches configuration information of delay element arrays set to a plurality of registers in a time sharing way and supplies to said delay means; and

said second switching means switches said plurality of clocks in a time sharing way and supplies to said delay means.

7. A semiconductor apparatus as set forth in claim 6, wherein said delay monitor circuit comprises a control means for controlling a power source voltage for supplying to said target circuit based on delay

information generated by a delay element array formed in a time sharing way.

8. A semiconductor apparatus as set forth in claim 7, wherein said control circuit compares a plurality of delay information generated by a plurality of delay element arrays formed in said delay means, and controls said power source voltage based on delay information with the largest delay ratio with respect to a clock cycle in a plurality of clock frequency domains.

9. A semiconductor apparatus as set forth in claim 8, wherein said plurality of registers are set a plurality of configuration information corresponding to the respective clock frequency domains.